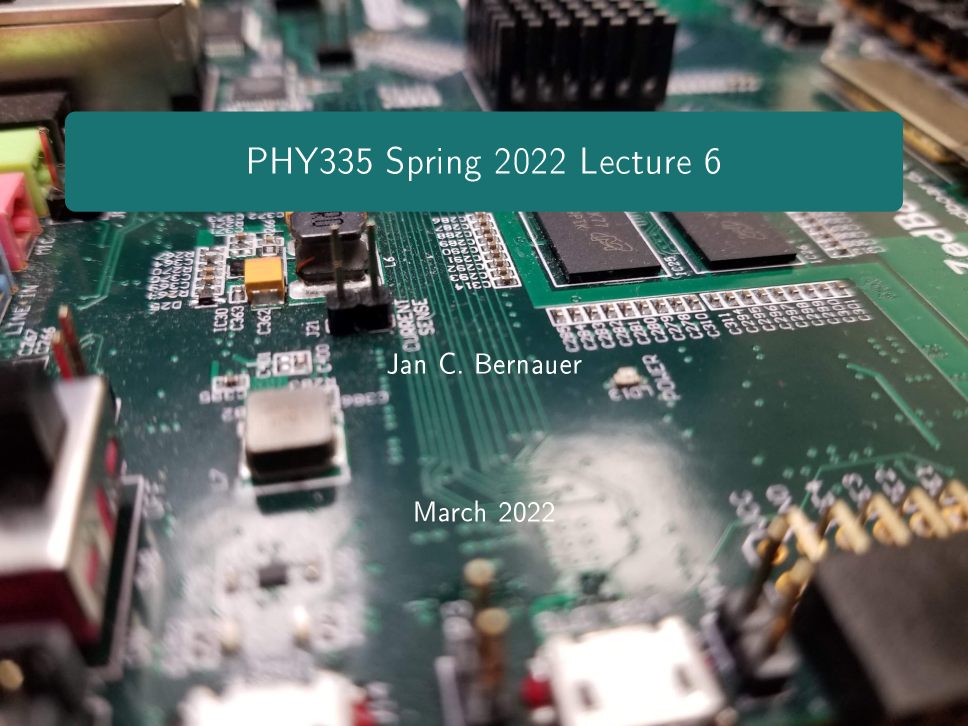
PHY335 Spring 2022 Lecture 6

Jan C. Bernauer

March 2022

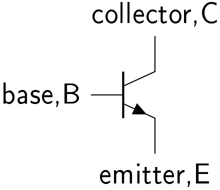


Transistor types

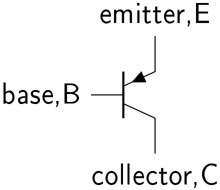
Generally: Three poles!

- BJT: Bipolar (junction) transistors: npn/pnp
  A current is controlled by a different current
- FET: Field effect transistors: n-channel / p-channel, (JFET, MOSFET etc.)
  A current is controlled by a voltage

BJT: npn / pnp

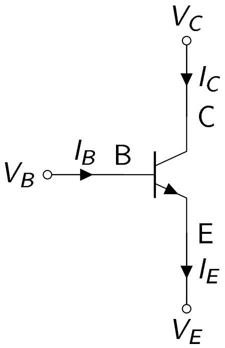


npn



pnp

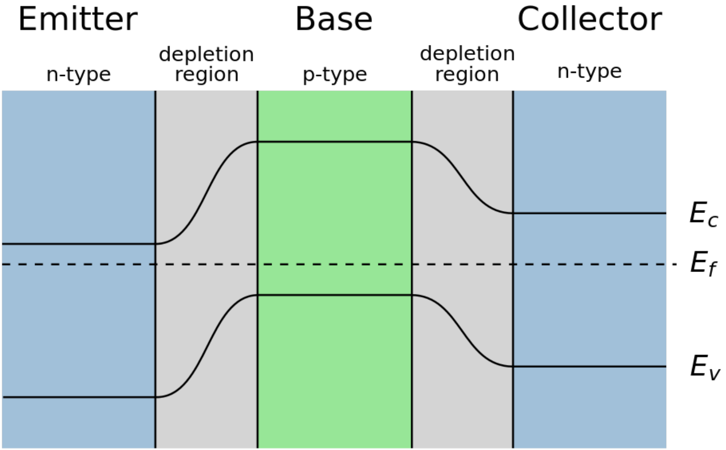
Nomenclature



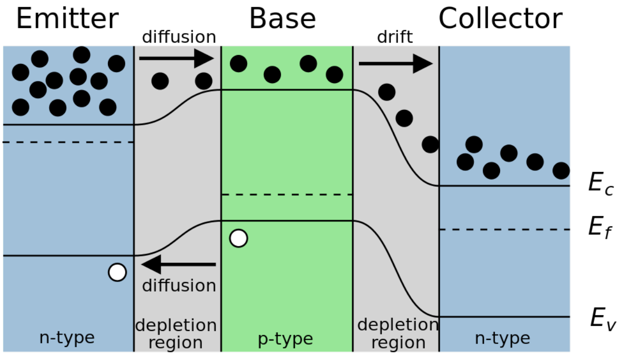
We are interested in voltage differences across the transistor:

- $V_{BE} = V_B - V_E$
- $V_{CE} = V_C - V_E$
- $V_{CB} = V_C - V_B$

Band diagram without voltages

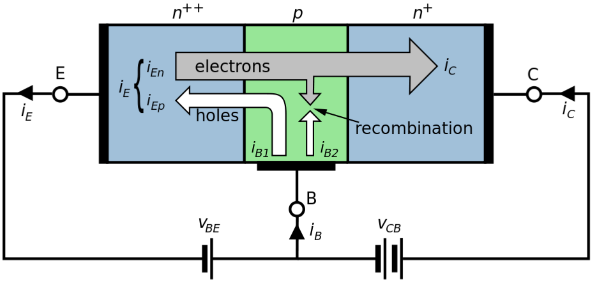


Band diagram in normal mode



- The BE levels are shifted so that electrons (majority carriers in n, minority in p) can travel into the base.
- At the BC side, the field from the reverse bias drifts the electrons out.
- The density gradient across the thin base drives electrons across it via diffusion

Operation modes



- Active: Base-emitter is forward biased ($V_{BE} > 0$), base-collector is reverse biased $V_{CB} > 0$. $I_C = \beta I_B$
- Reverse-active: Switch roles of C and E. Rarely used
- Saturation: $V_{BE} > 0$, $V_{CB} < 0$: maximum current
- Cut-off: $V_{BE} < 0, V_{CB} > 0$, both diodes in reverse, minimal current

Transistor rules for the "current model"

- Polarity: $V_{CE} > 0$

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- Maximum ratings: If you are outside, the magic smoke escapes.
- Then: Current amplifier: $I_C = h_{FE} I_B = \beta I_B$

β is a bad parameter: It can differ significantly for different specimen of the same type. (See datasheet)

Easy rule

$$V_{BE} \approx 0.6V$$

Or:

$$V_B = V_E + 0.6V$$

BJT current source

We want a constant current through a load, independent of the load impedance.

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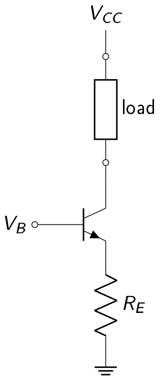

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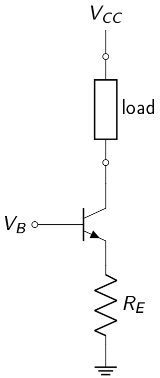

- $V_E = V_B - 0.6V$

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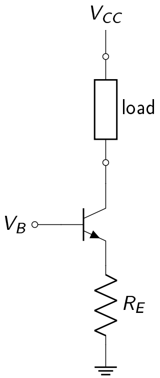

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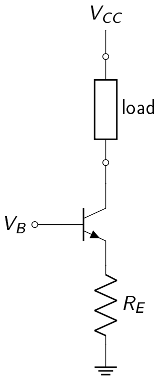

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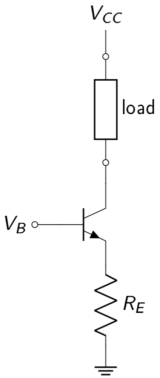

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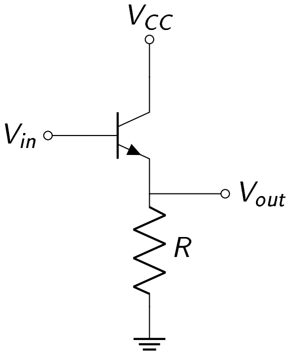
- $I_E = V_E/R_E$
- $I_{load} = I_C = I_E - I_B = I_E(1 - 1/(\beta + 1)) \approx I_E$
- So: $I_{load} = \frac{V_B - 0.6V}{R_E}$
- True as long as $V_E + 0.2V < V_C < V_{CC}$

Emitter follower



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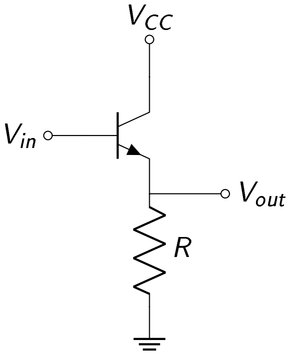
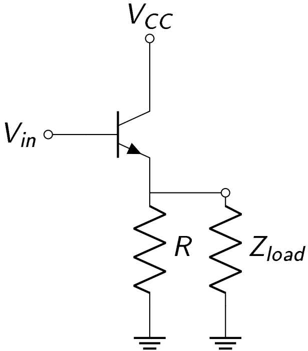


- $V_{out} = V_{in} - 0.6V$
- Feedback: "Signal" to transistor is $V_{BE} = V_B - V_E = V_{in} - V_{out}$

Input impedance



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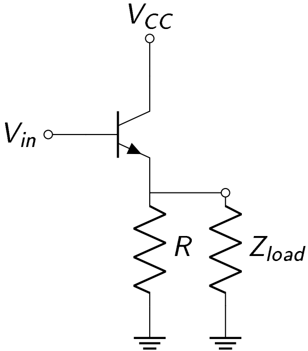

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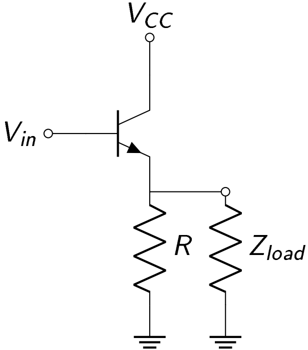

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$$\Delta I_B = \frac{\Delta I_E}{\beta + 1}$$

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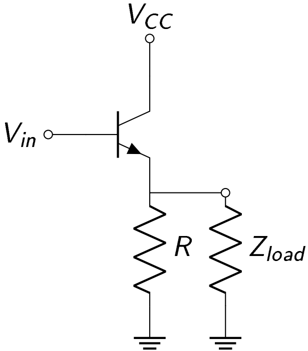

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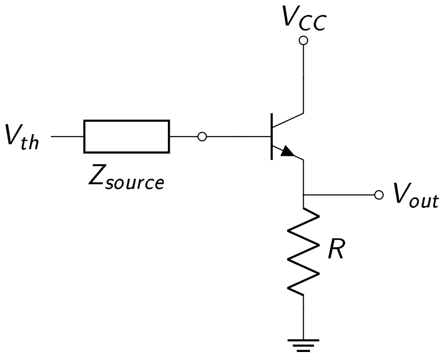
$$\Delta I_B = \frac{\Delta I_E}{\beta + 1}$$
$$r_{in} = \frac{\Delta V_B}{\Delta I_B} = (\beta + 1)(R \parallel Z_{load}) = \beta(R \parallel Z_{load})$$

Output impedance



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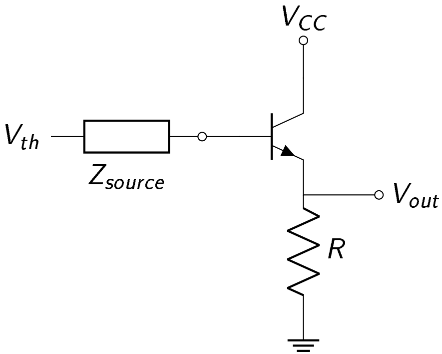
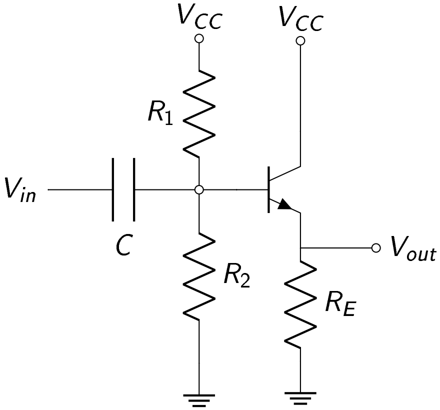


$$r_{out} = \frac{\Delta V_E}{\Delta I_E} = \frac{\Delta V_B}{(\beta+1)\Delta I_B} = Z_{source}\frac{1}{\beta+1} = Z_{source}/\beta$$

AC coupled emitter follower, working point



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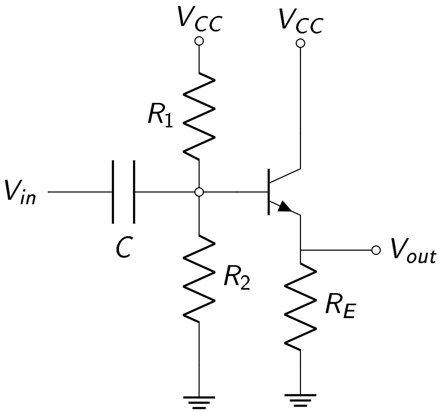

- We want the working point for $V_{out} = V_{CC}/2$ if we don't have an input, and we need to pick a bias current I_{bias}. This gives $R_E = V_{CC}/(2I_{bias})$

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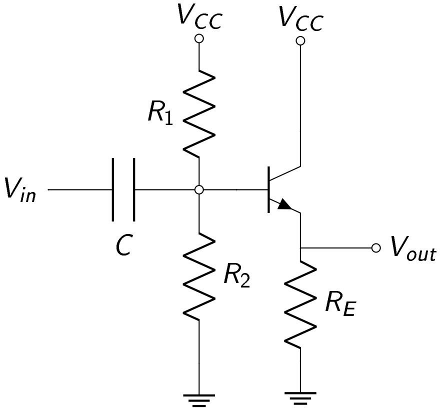

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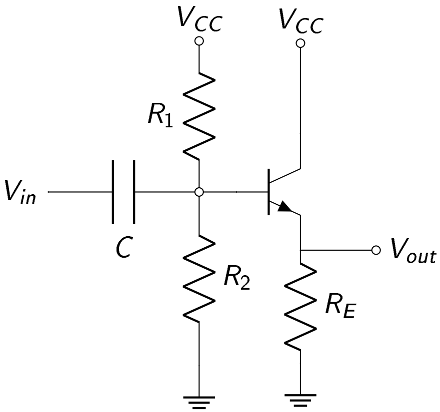

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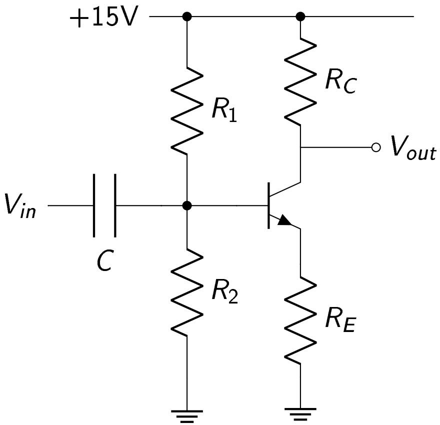
- We want $R_{1,2}$ large (to not load the source). But the divider is loaded by input impedance (see above). So, $R_1 \parallel R_2 < \beta R_E$

Common emitter amplifier



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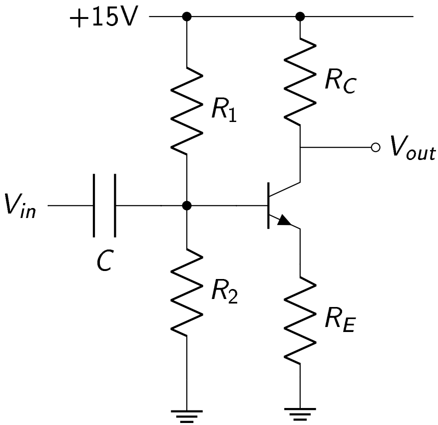

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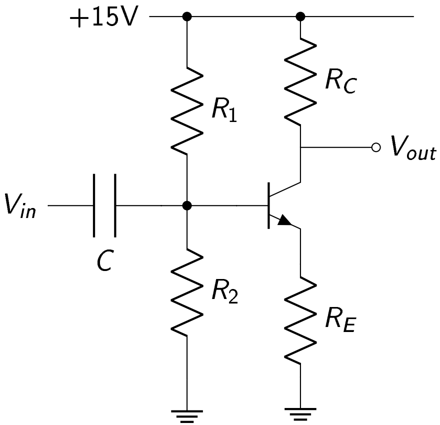

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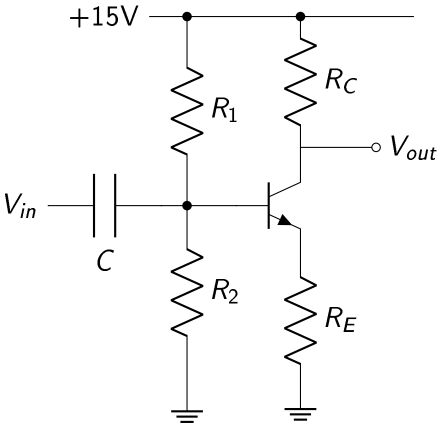

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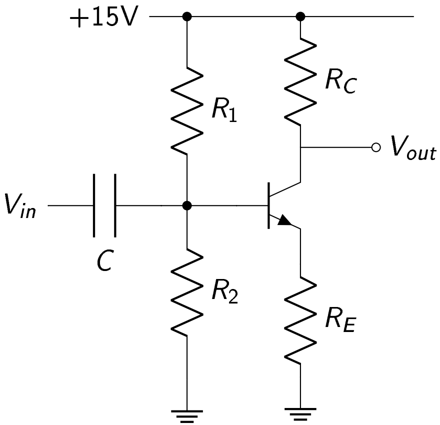

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- $v_{out} = v_C = -R_C i_C = -\frac{R_C}{R_E} v_{in}$

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- Input: Looking into the input (ignore the C), we see $R_1 \parallel R_2 \parallel \beta R_E$
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  - Current sources have (ideally infinite) large resistances, so R_C dominates and is the output resistance
- This means that R_C is limited by what ever we want to drive, and large amplifications need then very small R_E. How small can we make it?

No emitter resistor: Ebers-Moll equation

What happens if we omit the emitter resistor?

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- (As usual, we can mostly neglect the 1)
- A constant ΔV_{BE} gives a constant ratio $\frac{I_{E,2}}{I_{E,1}} = e^{\frac{e\Delta V_{BE}}{k_B T}}$

A closer look: r_E

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- $V_{BE} = \frac{k_B T}{e} \ln\left(\frac{I_E}{I_S(T)} + 1\right)$
- Linearize! We can find a small signal effective resistance:
  - $r = \frac{dV}{dI}$
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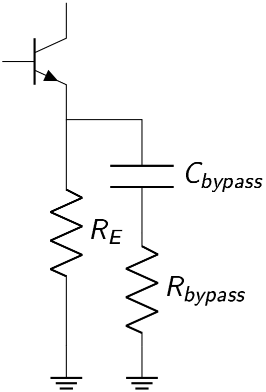
- This looks like an additional, intrinsic resistance on the emitter pole
- This limits the maximum amplification for the common emitter amplifier!

Small R_E

There is an additional problem with small R_E:

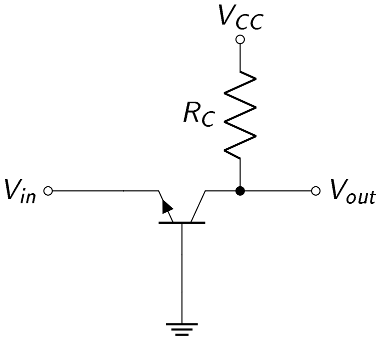
- Either the quiescent current is large $\Leftrightarrow$ Power dissipation
- Or V_E is small $\Leftrightarrow$ Large temperature drifts, since $\frac{dV_{BE}}{dT} \approx -2.1mV/^{\circ}C$

Bypassing R_E



- For the working point, at DC, a normal size R_E gives good temperature stability
- For a signal of relevant frequency, the C_{bypass} has small impedance. Then, the emitter resistance is $R_E \parallel R_{bypass}$, which can be very small

Common-base amplifier



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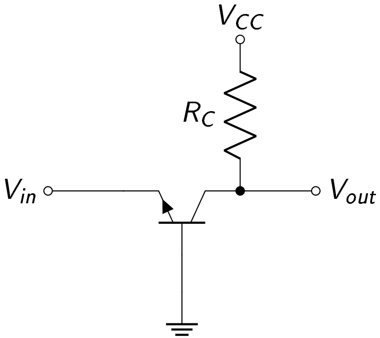

- $V_{in} < 0$
- Input impedance is very small: r_E
- This is good for current source-type of signals.
  - Many detectors are current sources, with some internal capacity.
  - Using a simple resistor to convert to voltage makes it slow
  - Transistor "hides" resistance, small $\tau = RC$

PNP instead of NPN

For PNP, reverse all polarities. Done.
Because now the current is carried via holes instead of electrons, they typically perform slightly worse.

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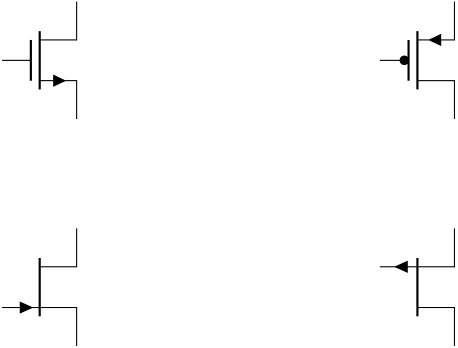
- Depletion or Enhancement mode

This gives 8 combinations, 5 are used, 4 are common: n/p-JFET dep. NMOS (enh/dep), PMOS(enh)

FET symbols



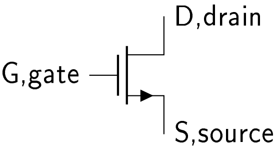
MOS

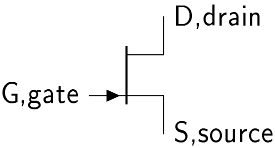
JFET

n-channel

p-channel

Nomenclature





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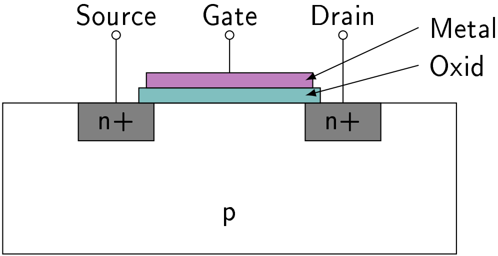
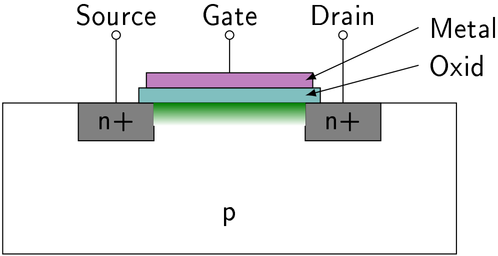


- with $V_{GS} \leq 0$, no conductance

MOSFET (n-channel, enhancement)

Remember the definition of resistance: $R = l/A \times \rho$. A FET modifies the area A of the conductive part!



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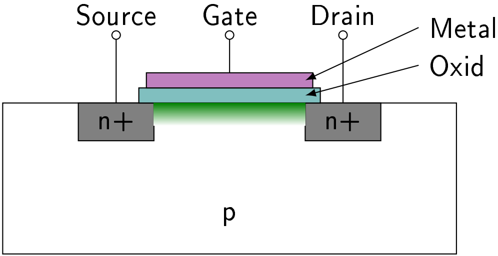

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- with $V_{GS} > 0$, the holes close to the gate are repelled, a inverted region forms
- A full channel forms for $V_{GS} > V_{threshold}$, a voltage V_{DS} can now drive a current.

- N.B: The D/S n and bulk p doped areas form a diode. It's important to keep this diode reverse biased. Often, the bulk is connected to the source, sometimes, it's available as a separate pin.

Operation modes: V_{GS} dependance

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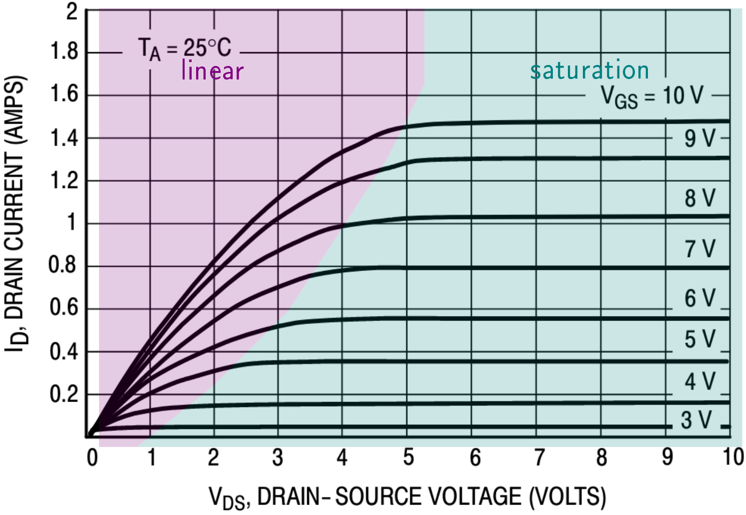
  - V_{DS} small: linear region

    $$I_D = 2\kappa\left[(V_{GS} - V_{th})V_{DS} - V_{DS}^2/2\right]$$

    Can interpret this as a voltage controlled resistor (but not quite ohmic)

    $$R_{DS} \approx \frac{1}{2\kappa(V_{GS} - V_{th})}$$

Operation modes: V_{DS}



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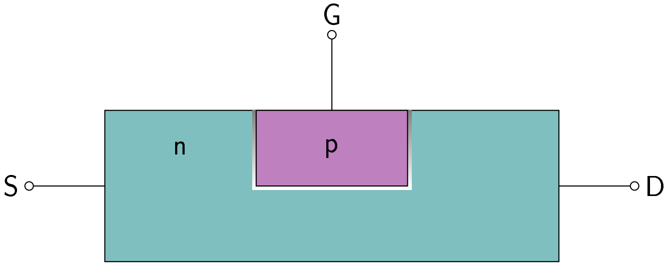
- One can even make V_{th} negative!
  - there is current flow possible even at $V_{GS} = 0$
  - have to drive V_{GS} negative to stop flow.
    $V_{GS}(I_D = 0) = V_P$ "pinch-off voltage"
- Junction FETs can only be in depletion mode

Junction FET (n-channel)



- $V_{GS} = 0$: Maximum channel width, maximum current, I_{DSS} (Drain current with gate Shorted to Source)
- NB: $V_{GS} > 0$ will quickly lead to large currents into the gate!

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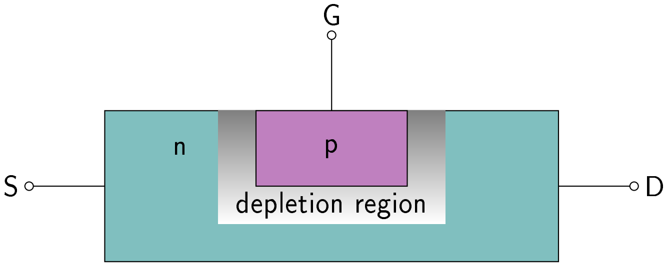
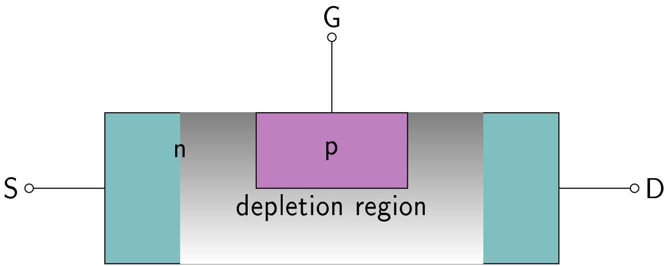


- $V_{GS} < 0$: Depletion region grows, makes channel smaller, $I_D < I_{DSS}$

Junction FET (n-channel)



- $V_{GS} \leq V_P < 0$: Depletion region pinched off channel, $I_D \approx 0$

Advantages / Disadvantages of FET

Good:

- No current on the controlling side, only voltage required
- In other words: infinite input resistance.
- No static power draw on the controlling side, can achieve small $R(on)$ on the controlled side

Bad

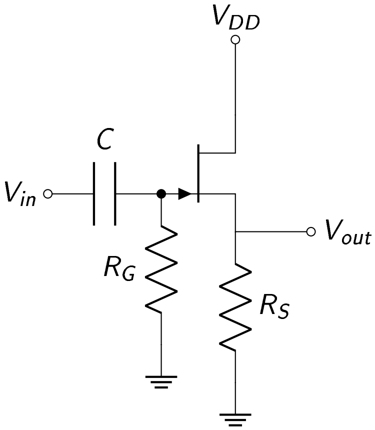
- Easy to destroy with static electricity
- Device parameters have a bigger scattering. E.g V_{th} and V_p have often a spread of 1-5V between specimen!

Basic FET circuits

- We can use the analog topologies of BJT
- Some circuits benefit greatly from FETs:
  - High-impedance/low current input: FETs need no current to operate, resistance in the order of $10^{14}\Omega$
  - Analog switches: see below
  - Digital logic: complementary MOS (pMOS and nMOS): no static power consumption
  - Power switching (MOSFET)
  - Linear circuits: Here, mostly JFET

Source follower

This is the equivalent of the emitter follower.



- JFET: depletion mode: conducting if $V_{GS} = 0$

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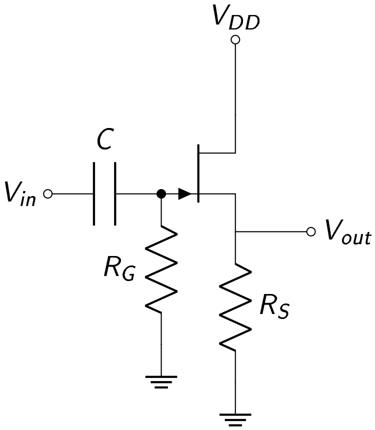

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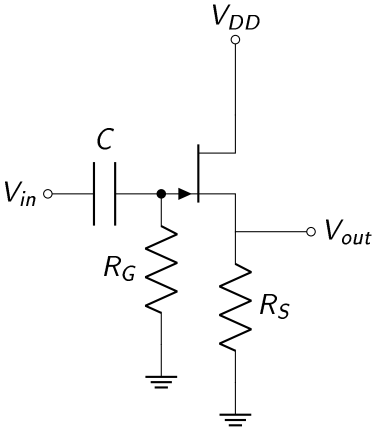

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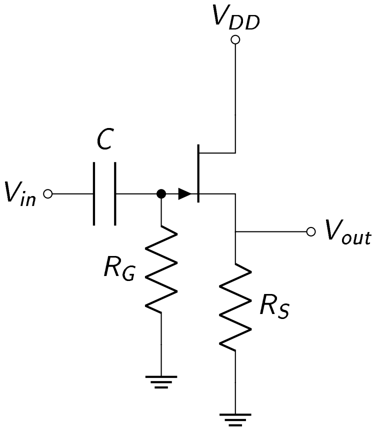

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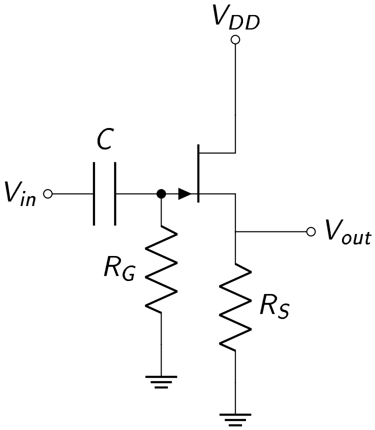

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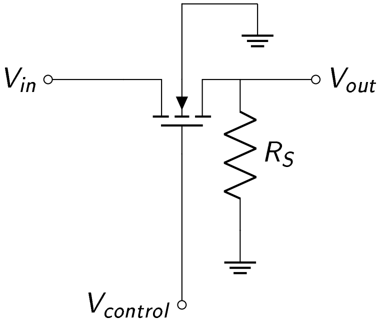
- Input impedance is dominated by R_G, which can be MOhms

Analog switch



- Enhancement mode MOSFET

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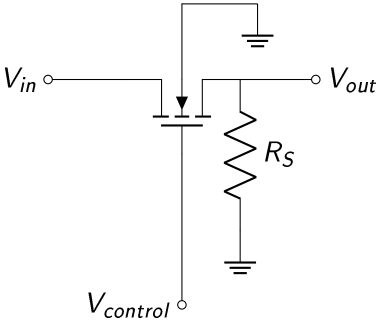

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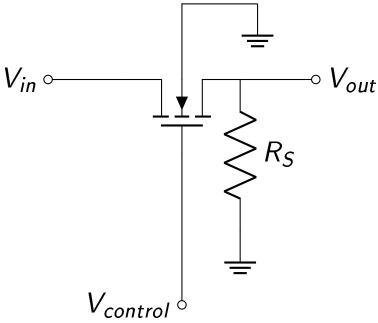

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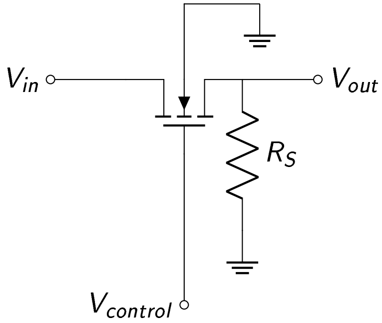

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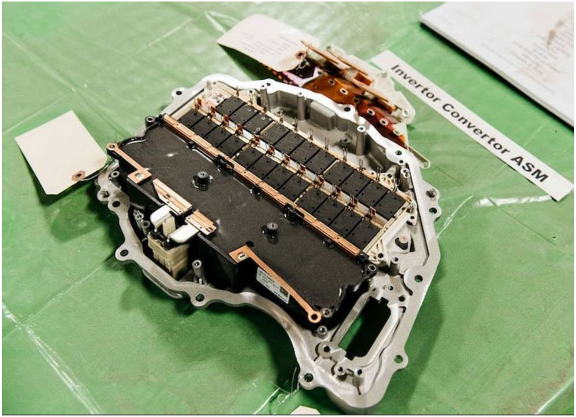
- if $V_{control} = V_{DD}$, all signals $0 < V_{in} < V_{DD}$ are passed through to V_{out}

Power switching

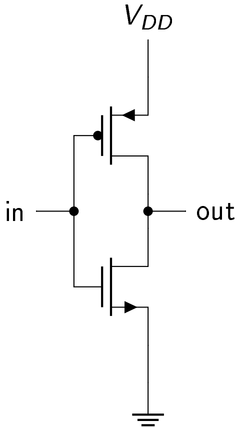


Model 3 inverter. Note two rows of rectangular devices

Taken from Motor Trend photos of Munro Ass. teardown

Each of the black devices can switch 100A at 650V....
$24m\Omega$ resistance when switched on

Logic: CMOS inverter



- A logic low input (0V) lets the upper FET conduct, which pulls the output to logic high (V_{DD})
- A logic high inout (V_{DD}) lets the lower FET conduct, which pulls the output to logic low (0V)
- Ergo: $out = \bar{in}$