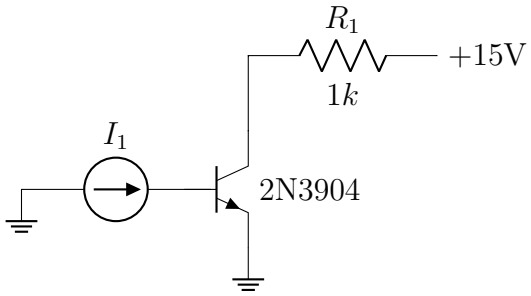
PHY 335, Unit 6 Transistors and transistor circuits

Mini Lecture topics:

- **p-n junctions re-visited**
- **How a bipolar transistor works**
- **Basic circuit rules for transistors**
- **BJT-based current source and its limits of operation**
- **Emitter follower design in detail**
- **Basic transistor circuits**
- **Effective collector resistance r_E in BJT**
- **JFET and MOSFET: types, principles of operation and characteristics**
- **Basic FET circuits**

1. Build the circuit below in LTspice and measure the current gain.

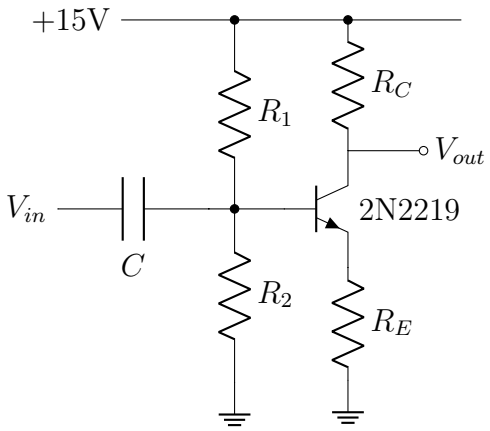


   - To select the transistor it LTspice, place a "npn" transistor. Right-click→Pick New Transistor for a selection box. Find the 2n3904.
   - In the datasheet, find the maximum collector current. With the resistor value in the schematic, what is the maximum voltage allowed for the voltage source?
   - Plot the current in the resistor as a function of the base current (current from the current source I1). To do so, tell LTspice to do a DC sweep simulation with these parameters: Name: I1, Type: Linear, Start: 0.01m. Stop: 0.5m, increment 0.0001.
   - Plot β, the ratio of the two currents. You can either export the simulation from LTspice, our use LTspice to plot the ratio directly: Right-click on the plot, Add Traces, Expressions to add: I(R1)/I(I1)
   - In the plot, identify the active and saturation region.
   - Comment on the determined value of β in the active and in the saturation region.

2. Emitter Follower: Design, build and test an AC-coupled emitter follower circuit using 2N 2219 BJT or a similar BJT.

   - You have to pick suitable resistor values to set the working point. Aim for an emitter current of about 5 mA at the working point (constant or no input signal). At the working point, the emitter voltage should be $V_{CC}/2$, in our case 7.5V ($\pm$0.5V or so). This sets your R_E. Explain why the centering of V_E is desirable (hint: think about what happens with large input amplitudes).
   - To achieve 5mA emitter current, you have to bias the base accordingly. Knowing V_E, you can estimate V_B, and from that calculate the voltage divider ratio. Further, choose biasing resistor values so that the DC bias of the base remains fixed to within 10%. To achieve this, consider the Thevenin equivalent of the base biasing voltage divider, and also consider the effective input resistance of the transistor base. For the latter recall the follower's main useful function, and assume current gain β of 100.
   - In this particular design the signal is coupled to the base through a capacitor to exclude DC shifts and/or slow signal level drifts (this is not necessarily so in all followers, but in this case, we want to have an AC coupled signal). Having this capacitor creates a high-pass filter at the input. This can further help to exclude unwanted low frequencies. For example, if we know that the signal frequency will be always higher than, say, 300 Hz, we can exclude 60 Hz interference. Choose the AC coupling capacitor so that –3 dB low frequency cut off of the effective RC filter is at about 300 Hz. Think very carefully about what effective resistor value should be used in this calculation. Draw the circuit, show all calculations, label the elements (R's, C) and build the circuit.
   - Measure and record all DC voltages at the three transistor terminals. Drive your follower from the function generator and observe the input and the output signals on the scope. If your follower works properly, you will see identical signals, shifted by about 0.6 V. This by itself is not very impressive. How can you prove that the follower indeed performs its main function of greatly increasing the effective load (emitter) resistance? Hint: Try to drive the same load without a transistor, keeping all the other circuit elements the same (namely, keeping the same voltage divider). Do you see the difference? Record the results, and compare them to what you get using a follower. Using the 2 V p-p signal from the signal generator(SG), measure and plot V_{out}/V_{in} vs. log(f) from 100 Hz to 1 MHz.
   - Set f = 10 kHz, and vary V_{in} from 2 V to 20 V p-p. Measure Vout and explain what you see. Again, think about the reason we chose quiescent emitter voltage at about $V_E \approx V_{CC}/2$.
   - Does the emitter follower have feedback? Explain how.

3. Build a BJT common emitter amplifier



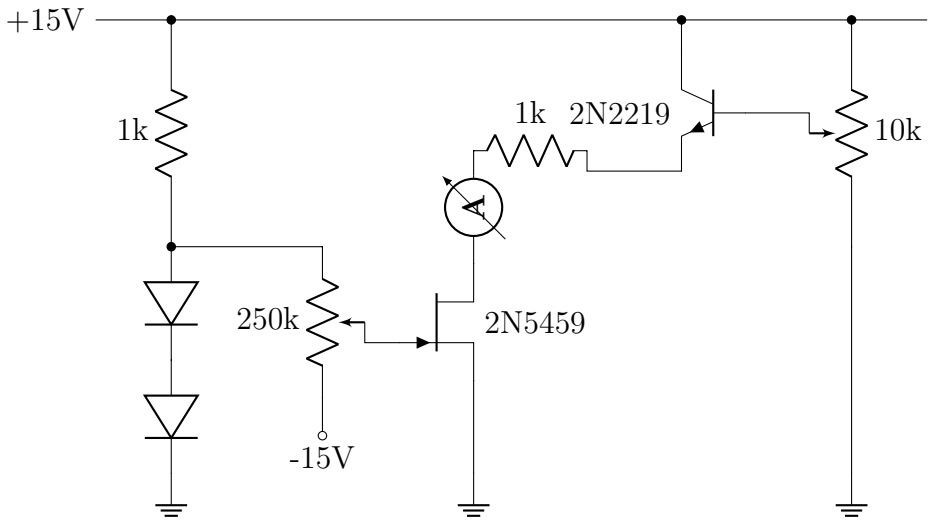
Design a common emitter amplifier with the following parameters.

- $V_{CC} = +15V$
- Output centered at 7.5 V
- Voltage gain of 20dB
- Quiescent current of 0.5 mA
- -3dB frequency 200 Hz.

Aim at being at least 15% within these specs. Ignore the temperature stability issues outlined in AoE.

- Explain the working principle based on transistor rules, derive the formula for voltage gain. Does the amp have feedback? Describe in details how you designed your amplifier, with all the calculations shown. Explain why the divider looking into the base must be quite asymmetric here, while it is almost symmetric in the emitter follower.
- Test your amp at different frequencies below 200 Hz and much greater than 200 Hz (several kHz) with sinusoidal input signals. Make sure to provide small enough input. It will be multiplied by 10, and you want to avoid violating the transistor rules. Is the output the same polarity or inverted compared to the input? Think of the role of the RC filter at the input. Will this filter produce a phase shift at high frequency? Is the output shifted up by 7.5 V? What if you increase the input so that the output amplitude becomes greater than 7.5 V. Describe what happens. Sketch what you see on the oscilloscope.

4. FET characteristics. Wire the following circuit to measure JFET characteristics.



Circuit Notes:

(a) This circuit allows measuring transistor characteristics: I_D as a function of V_{GS}, and I_D as a function of V_{DS}.

(b) The indicated JFET has an n-type channel and p-type gate. This means that the gate-source would be forming a forward-biased p-n junction at gate voltages higher than the normal diode drop of about 0.6-0.7 V. Thus we can not apply positive potential to the gate significantly over that value, or the gate-source junction will conduct large current into the transistor. As a result of the above consideration, in this circuit we use two diodes making a clipping circuit and thus limiting positive voltage from the divider to about 1.4 V, so that the divider can deliver from –15 V to +1.4 V. We will need only a few negative volts to pinch off the transistor (see the transistor datasheet)

(c) The emitter-follower which you built previously is used here to increase the impedance and to allow a second voltage divider to deliver full voltage to the JFET's drain. This will be used to change V_{DS} in measuring I_D vs. V_{DS}.

- Determine the pinch-off voltage (also called gate-source cutoff voltage) V_P, defined as the voltage at which the current drops to about 1 μA. Compare what you found with the datasheet values.
- Determine I_{DSS} for $V_{GS} = 0$ at the highest V_{DS} you can get with your setup (up to +15V). You can short the gate to the ground, or dial zero volts from the divider. As before, compare your results with the device specs.
- With V_{DS} still at the highest value, plot the relationship between I_D and V_GS from $V = V_P$ (a few volts negative) to about V = 0.7 V positive.

- Plot the relationship between I_D and V_{DS} up to the highest V_{DS} you can get with your setup. Do this plot once for $V_{GS} = 0V$ and once for a V_{GS} that gives you a current $I_D = 1mA$ on the plateau (i.e., at large V_{DS} values). This current occurs at some V_{GS} between V_P and V=0. Show that at low voltages the transistor behaves as a voltage-dependent resistor. Plot this part of the two curves on an expanded scale separately. Calculate resistor values for the two curves. Calculate the FET's transconductance (in Siemens or inverse ohms (often written mhos)) for the two V_{GS}